Foreword

The MBI6027 is a constant current LED driver for RGB cluster applications. The stability of data transmission has been improved through clock reverse and A-Token™ topology. This article mainly addresses five parts:

I.The module design, LED and gray scale setting…etc.

II.The controller signal design, including configuration mode, the installation timing… etc.

III.The production and setup, including the effect of hot swap, the connector design of how to reduce the surge voltage when clusters are installed or removed…etc.

IV.The method of system testing.

V.Other applications notice, such as high V_{LED} application.

I. Module Design

Figure 1 is the MBI6027 application circuit.

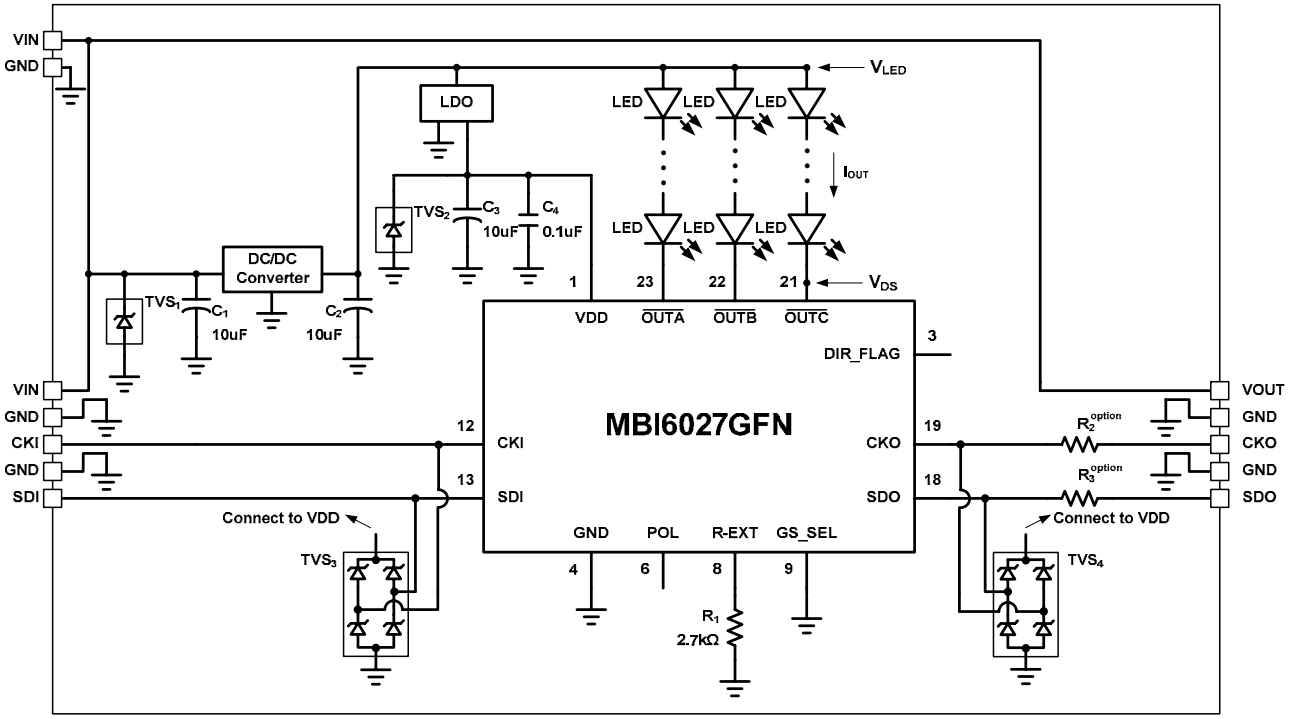

Figure 1. MBI6027 application circuit

1. Notice About LED

The higher V_{LED} may result in high voltage drop on MBI6027's output port while adopting LEDs with large variation of forward voltage and then cause overheat. Therefore, LED forward voltage (V_F) sorting is necessary.

2. Setting Gray scale bit

The gray scale bit will be set through the GS_SEL when connects the GS_SEL to GND. The gray scale of MBI6027 will be set to 12-bit, as Figure 2 shows. If the GS_SEL pin connects to VDD, the gray scale will be 8-bit.

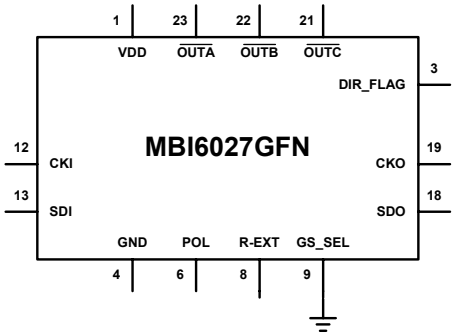

Figure 2. The schematic of GS_SEL connecting to GND

3. Setting Current Notice

MBI6027 allows users to set three LED current (I_{OUT}) by an external resistor, R_1. After setting the LED current, users can get a suitable R_1 by the following equations.

$$R_1 = (0.617V / I_{OUT}) \times 23 \quad \text{..... (1)}$$

R_1 must be placed close to MBI6027 in order to prevent R_1 from being disturbed. Moreover, the 1% tolerance resistance is recommended to obtain the accurate output current.

To keep MBI6027 at constant current, a sufficient voltage at $\overline{OUTA}$, $\overline{OUTB}$ and $\overline{OUTC}$ of MBI6027 (V_{DS}) is needed. Figure 3 and Figure 4 show the I-V curves of MBI6027. Users can refer to the Figures and get a suitable V_{DS}. In general, the V_{DS} is slightly greater than the knee voltage. (Recommendation: V_{DS} = V_{knee}+0.2V)

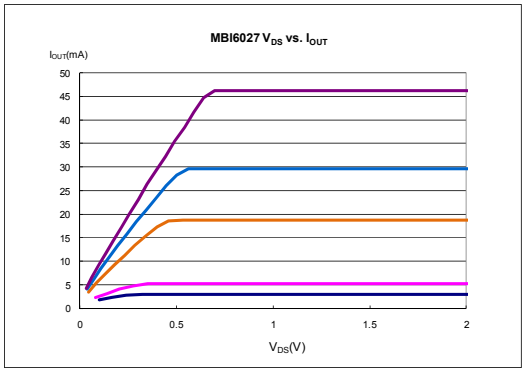

Figure 3. the relationship between I_{OUT} and V_{DS} of VDD=5V

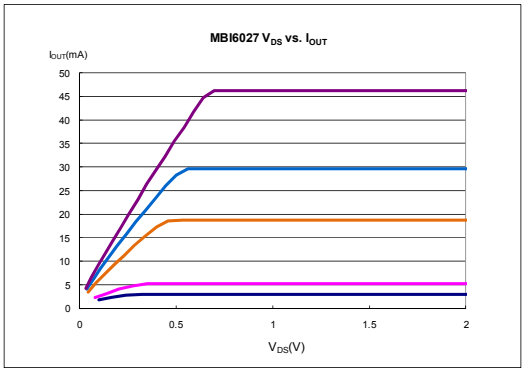

Figure 4. the relationship between I_{OUT} and V_{DS} of VDD=3.3V

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Table 1. The reference table of I_{OUT} and V_{knee}

I_{OUT}	R_1	Knee Voltage (V_{knee})
5.2mA	2.7kΩ	0.3V
10mA	1.3kΩ	0.4V
20mA	710Ω	0.5V
30mA	470Ω	0.6V
43mA	330Ω	0.7V

When doing the PCB layout, please keep the layout traces of $\overline{OUTA}$, $\overline{OUTB}$, $\overline{OUTC}$ and R-EXT away from the CKI/SDI/CKO/SDO to avoid the interference of crosstalk. Or it is recommended to use the ground plane to separate these wires shown in Figure 5.

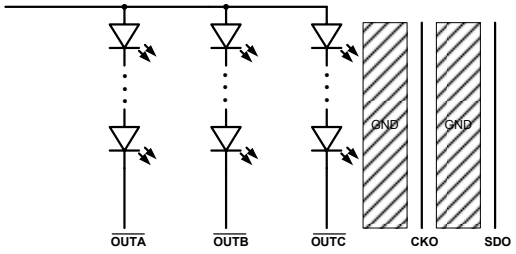

Figure 5. Use the ground plane to isolate CKI/SDI/CKO/SDO and $\overline{OUTn}$

4. Setting LED Power

The minimum V_{LED} can be determined by the following equation

$$V_{LED,\ MIN.} = (V_{F,\ MAX.} \times n) + V_{DS} \quad \text{..... (2)}$$

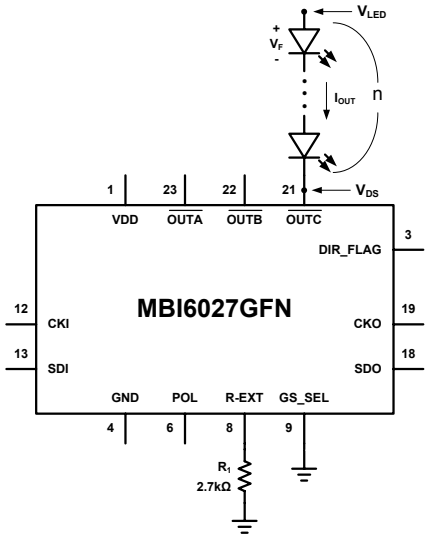

Figure 6. The sketch of minimum V_{LED} voltage

where $V_{F,MAX}$ represents the maximum forward voltage of LED, and n is the number of cascaded LEDs. The maximum sustaining voltage of $\overline{OUTn}$ is 17V. If the supply voltage of LED (V_{LED}) is over 17V, the IC will be damaged. For the higher V_{LED} application, please refer the P.21.

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5. Power Configuration

Because of the impedance of power lines, the voltage of each cluster might be different in the multi-cluster cascaded application as shown in Figure 7. Users have to calculate the dropout voltage caused by the impedance of power line. For example, the biggest conductor impedance of AWG26 (Maximum Conductor Resistance) of UL1007 is 152Ω/km. It means that 1km transmission line is equal to 150Ω. When transmission line is 50cm and current is 20mA, there will be 1.52mV voltage drop. When the voltage is lower than that of DC/DC converter supply voltage, users should use a new power line, as shown in Figure 10 and Figure 11.

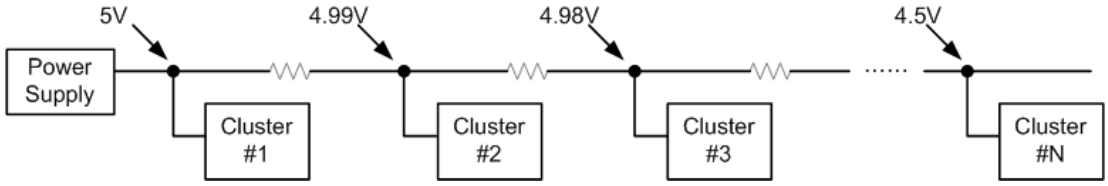

Figure 7. The sketch of dropout voltage in multi-cluster cascaded application

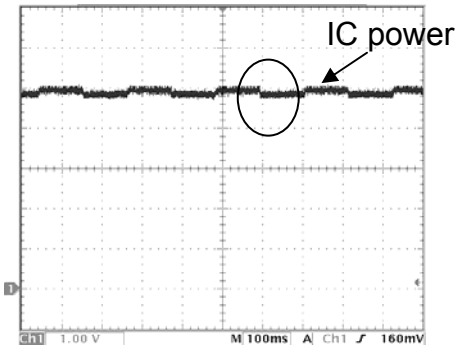

Figure 8. The poor waveform of power

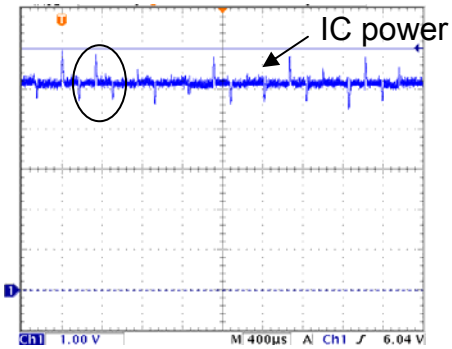

Figure 9. The poor waveform of power

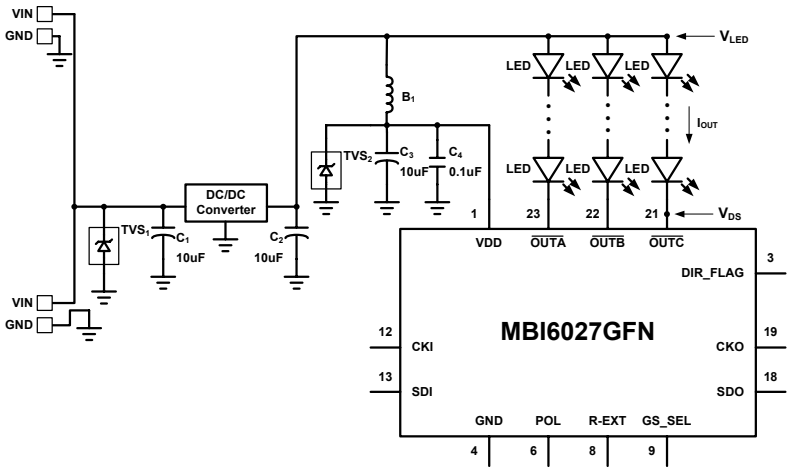

Figure 10. The proposed method of the power

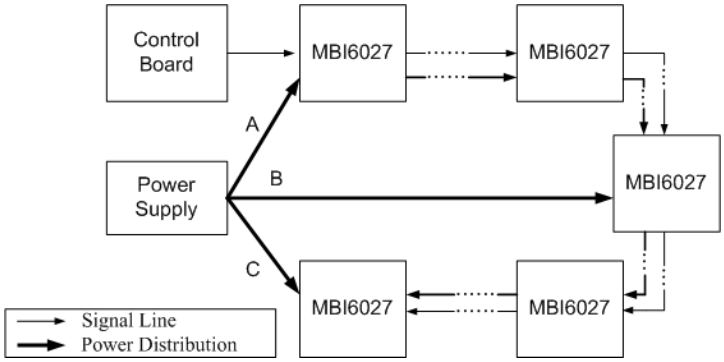

Figure 11. The power distribution of clusters

Table 2. The specification of transmission line

UL 1007 / CSA TR-64	Range		Conductor		Insulation		Tolerance mm	Maximum Conductor Resistance Ω/km	Permitable Current A	Minimum Insulation Resistance MΩ/km	(VAC/min) Insulation Potential Strength
	Temp ℃	Voltage V	AWG	NO./MM	Thickness mm	O.D. mm					
Stranded	UL 80℃ CSA 90℃	300V	32	7/0.080	0.38	1.00	±0.10	703	1.6	15	2000
			30	7/0.100	0.38	1.10	±0.10	397	2.0		
			28	7/0.127	0.38	1.20	±0.10	248	2.5		
			26	7/0.160	0.38	1.30	±0.10	152	3.5		
			24	11/0.160	0.38	1.45	±0.10	88.6	5.0		
			22	17/0.160	0.38	1.60	±0.10	62.5	7.0		
			20	21/0.180	0.38	1.85	±0.10	39.5	9.0		
			18	34/0.180	0.38	2.10	±0.10	24.4	13.0		
			16	26/0.254	0.38	2.40	±0.10	15.6	17.0		
Top-Coated(ATC)			30	7/0.100	0.38	1.10	±0.10	397	2.0		
			28	7/0.127	0.38	1.20	±0.10	248.0	2.5		
			26	7/0.160	0.38	1.30	±0.10	152.0	4.0		
			24	7/0.200	0.38	1.45	±0.10	88.6	5.3		
			22	7/0.254	0.38	1.60	±0.10	62.5	7.2		
Solid(TA)			26	1/0.404	0.38	1.25	±0.10	155	3.8		
			24	1/0.511	0.38	1.40	±0.10	92.4	5.3		
			22	1/0.643	0.38	1.55	±0.10	60.1	7.2		
			20	1/0.813	0.38	1.70	±0.10	37.0	9.4		
			18	1/1.020	0.38	1.96	±0.10	23.6	13.0		

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6. Signal Quality

Good waveform quality should be no crosstalk , no overshoot/undershoot and the amplitude of the voltage is higher than V_{IH}. Figure 12 describes the signal waveform with good quality.

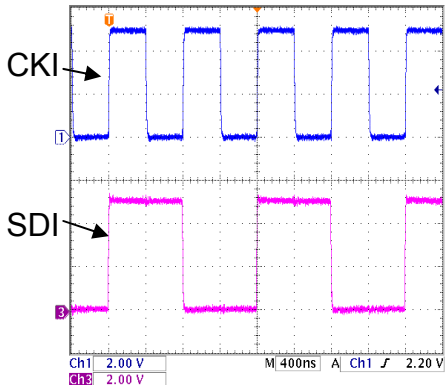

Figure 12. Good quality signal waveform

6.1 Cross-talk

When two signal lines are juxtaposed together, a phenomenon will happen on these two signals, as shown in Figure 13. In order to suppress the cross-talk, a GND line to separate these two signals is necessary, as shown in Figure 14. A twist pair cable is easy to suffer cross-talk. Therefore, it is not suggested to adopt the twin wires in this application.

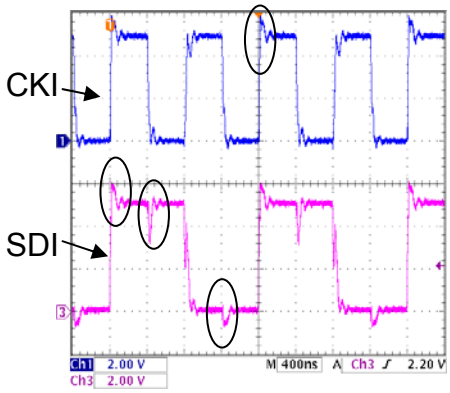

Figure 13. The waveform of cross-talk

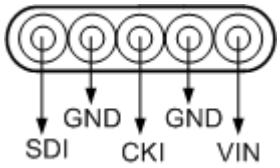

Figure 14. The arrangement of transmission line

6.2 Overshoot/Undershoot Voltage

Figure 15 shows the overshoot and undershoot voltage on CKI and SDI signals. In order to improve the signal quality, it is recommend to reserve the PCB positions of R_2 and R_3 in Figure 16 The resistance of R_2 and R_3 will affect the rising and falling time of CKO/SKO. The larger resistance results in slower rising/falling time and reduce the effect of over/undershoot voltage. However, the large resistance might cause abnormal transmission.

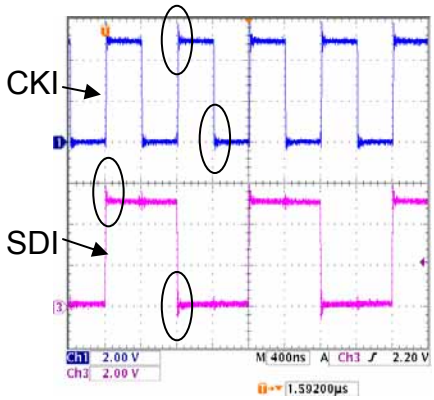

Figure 15. The poor waveform of overshoot or undershoot voltage

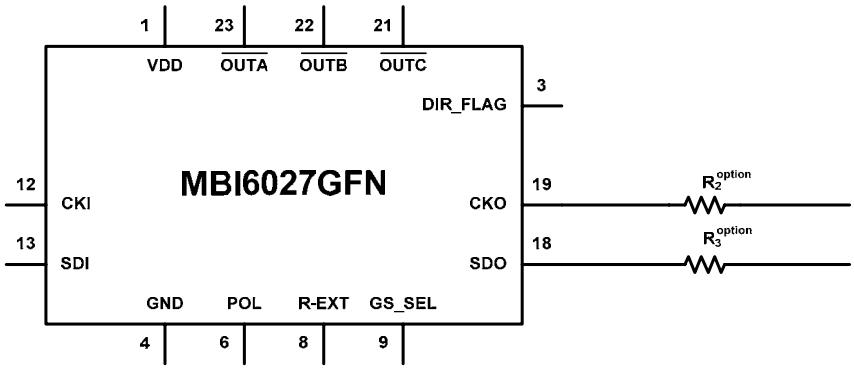

Figure 16. The sketch of how to improve the poor waveform

6.3 Amplitude

The factors that affect amplitude include equivalent capacitance of wire, equivalent capacitance of TVS, voltage of VDD and resistance of CKO/SDO. User can choose shorter wire to reduce the equivalent capacitance and smaller equivalent capacitance of TVS and adjust resistance of CKO/SDO.

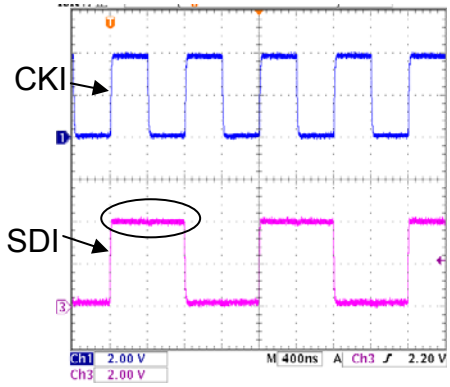

Figure 17. The poor waveform of insufficient amplitude

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II. Control Signal Design

1. Configuration Mode

The two times prefix of configuration mode must be larger than 250us. The data needs to be adjusted based on real situation. In addition, in order to avoid a sudden power interruption (ex: lightening stroke, power failure ... etc) within a fixed time, users can write into configuration mode as shown in Figure 18.

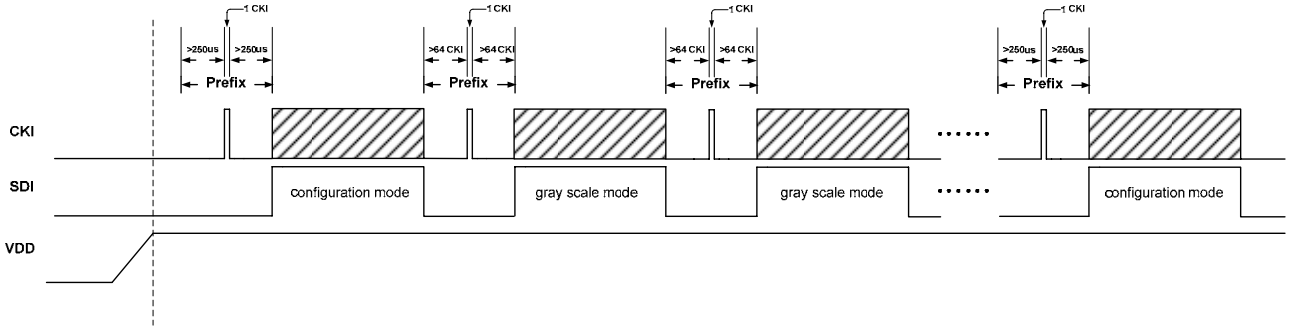

Figure 18. The sketch of configuration mode

2. Design Installation Timing

Users usually use a simple frame to check if the transmission line and module work normally in installation. However, this process will cause MBI6027 into error mode. Therefore, MBI6027 should be continue into the configuration mode, dot correction mode and gray scale mode. Figure 19 is the timing diagram of system installation. Please refer to page 13~15 for the prefix time of configuration mode which must be larger than 250us and be input twice.

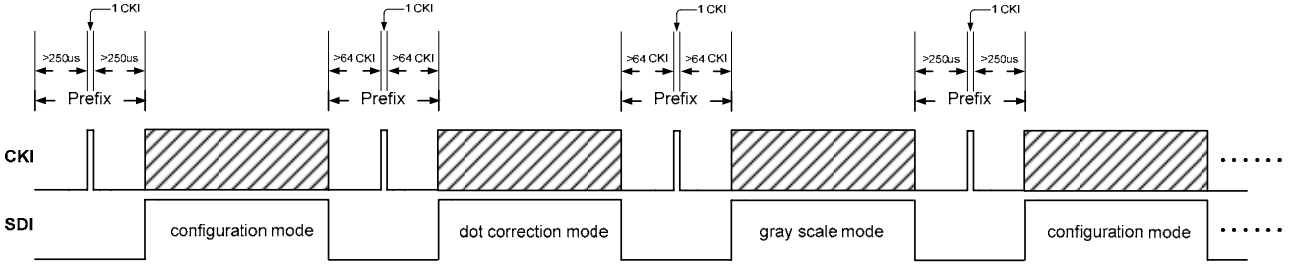

Figure 19. The timing diagram of system installation

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3. Notice for Controller

For the engineering test, please add a switch on the controller to switch the processes of system installation and general frame. To improve the validity of control signal, the control signal should be output after the power supplies of controller and module are stable and use the circuit of power on reset to initialize MBI6027. The transmission lines of CKI and SDI from controller to first cluster should be separated by a ground line and add a GND on connector to be the common ground.

4. CKI Frequency Notice

The minimum CKI frequency of MBI6027 is 200kHz. Users should use fixed CKI frequency to improve system stability.

5. CKI Stop Time

The time-out protection of MBI6027 is to check the validity of data counter by counting the period of CKI stop through the internal counter. If the stop time of CKI exceeds 2 successive times of 8 CKIs, MBI6027 will ignore the present input data and keep the previous frame data until the next correct data is input. Users should avoid above situation.

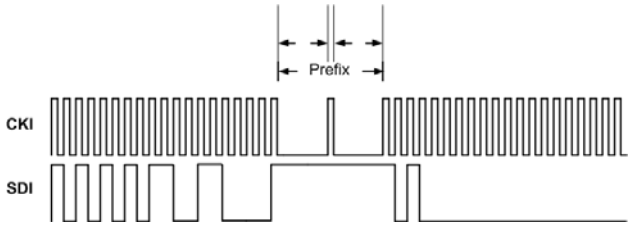

Figure 20. Diagram of time-out

6. Input Signal

The output signal of controller should allow the falling edge of CKI in the middle of SDI data. The recommended CKI is 50% of the duty, as shown in Figure 21.

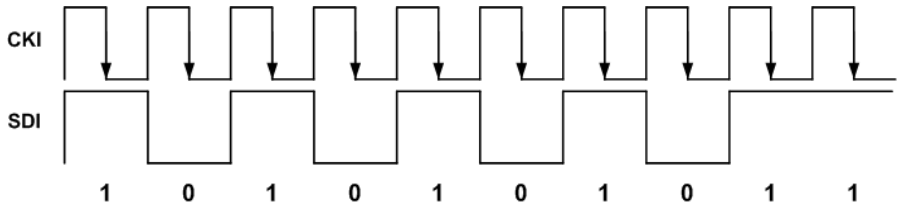

Figure 21. The falling edge of CKI in the middle of SDI data

The correct input signal format should consist of Prefix, Header and Data.

Figure 22. The correct input signal format

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6.1 Prefix

The prefix is the time that the CKI and SDI pull low (T_{d0}) simultaneously. In order to make MBI6027 realize recognizes the new header and meet the image refresh time (T_{frame}), the following equations can be used to calculate the prefix.

$T_{d0} \leqq (T_{frame} - T_{D0}) / 2$ ..... (3)

$T_{d0} > 64 \times CKI\ period$ ..... (4)

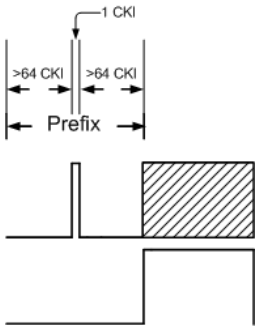

Figure 23. The diagram of Prefix

where T_{D0} represents the time of transmission, T_{D0} of 12-bit is T_{CKI} x (48 + 36 x N) and 8-bits is T_{CKI} x (48 + 24 x N). N is the amount of cascaded IC and T_{CKI} is the CKI period, as shown in Figure 24.

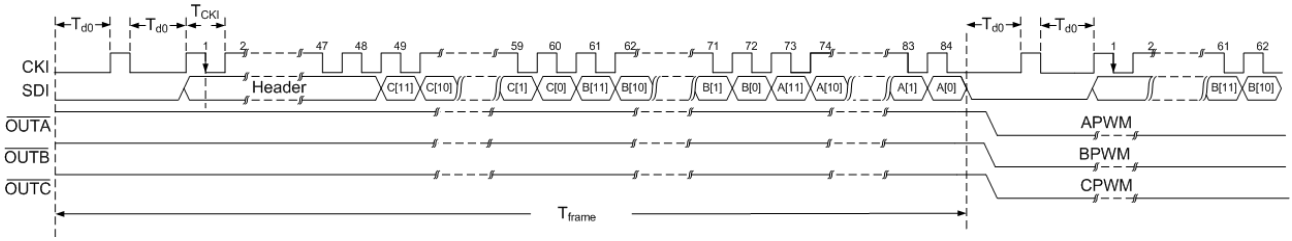

Figure 24. Diagram of prefix

Example

Number of MBI6027 in cascade: 256 pcs,

Gray scale data:12-bit,

CKI time-out period: 64 CKI,

Period of CKI (T_{CKI}): 1us (1/1MHz),

Refresh time of a frame: 16.67ms (1/60Hz).

From equation (3), T_{d0} = [16.67ms - 1us x (48 + 36 x 256)]/2 = 3.703ms. The time is larger than the time of 64 x 1us = 64us. The data stream can be recognized, as shown in Figure 25.

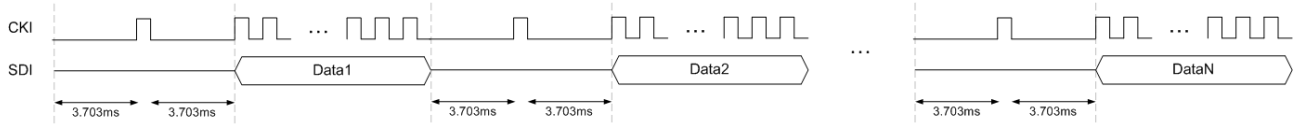

Figure 25. The Diagram of Prefix is 3.703ms

6.2 Header

The correct header must be transmitted before the gray scale data to make sure each MBI6027 can catch the gray scale data with correct address. The header includes Preamble, CMD(Command), A(Address), L(Length) and P(Parity Check).

Preamble Illustration

Preamble is used to identify the Header. Users must fill 16'b1010101011001100 in Preamble position.

Command Illustration

Command is used to identify the modes. Users select mode in accordance with the implementation of the corresponding Command. Table 3 is Command of the corresponding table.

Table 3. Command of the corresponding table

CMD[31:24]	CMD Type
8'b 0010 0011	Configuration mode
8'b 0001 0011	Dot correction mode
8'b 0011 1111	Gray scale mode
8'b 0001 0100	Software reset mode
8'b 0010 0000	IC status read mode
8'b 0110 0011	Configuration with status read mode
8'b 0101 0011	Dot correction with status read mode

Address and Length Illustration

A-Token™ is the address setting method of MBI6027. The theorem of A-Token™ is to distribute the A(Address) and L(Length) to each IC automatically. The address data will be added by 1 whenever the data chain pass to the next IC, and the Least Significant Bit (LSB) will be exported first to address the next IC. When the data of A(Address) and L(length) are the same, the data will be latched to register. **The L(length) of MBI6027 is the amount of cascaded ICs minus one.** For example, if there are three MBI6027 in cascaded, the L(Length) will be 2(10'b0000000010), and **the initial A(Address) is 0(10b'0000000000).**

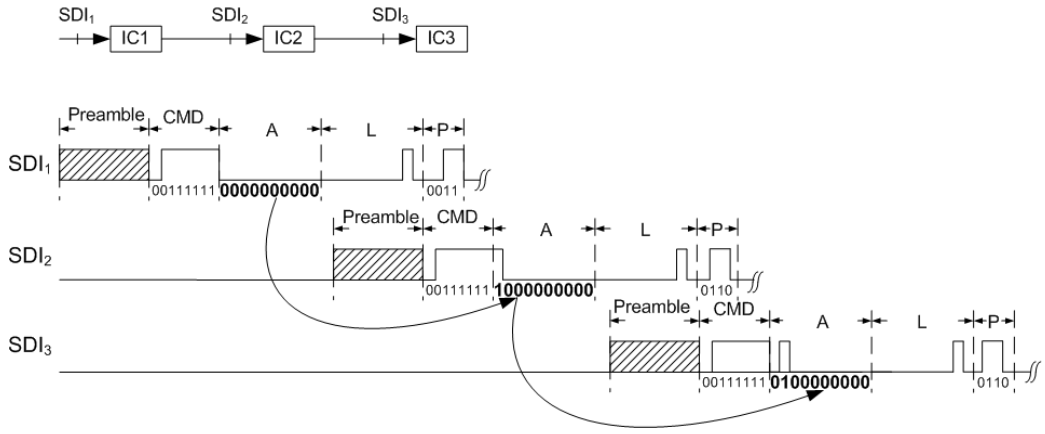

Figure 26. Diagram of A-Token™(gray scale mode)

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Parity Check Illustration

The parity check function is to check if there is any error data in the Command, Address and Length. If the count of parity is incorrect, it shows that the Command, Address or Length, and the data chain will be invalid and the IC will keep the previous frame data until the result of parity check is correct. The example of parity check shows as below. The P[0] of parity check is the odd/even result of P[3:1], as shown in Figure 27.

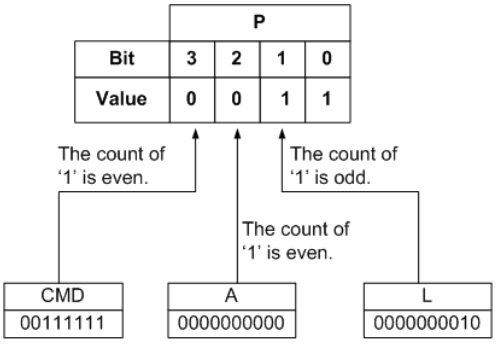

Figure 27. The example of parity check

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Following shows the example of three MBI6027 in cascade with different commands

Configuration Mode

Configuration mode is to set the current gain. When the IC power is on, the current gain will be recovered to 255 (default). Users must execute the configuration mode before the gray scale mode. Figure 28 is the timing diagram of configuration mode.

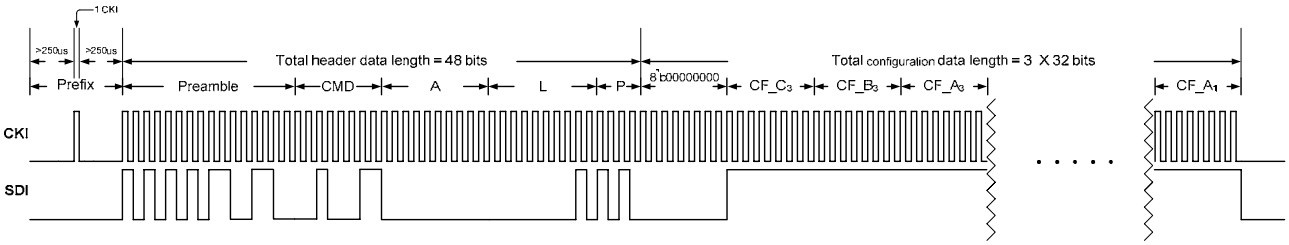

Figure 28. The timing diagram of configuration mode

The prefix time must be larger than 250us and be executed two successive times; the CMD[31:24] must fill in 8'b00100011. And since the L[13:4] is 2 (10'b0000000010), the data length of configuration data is 3x32 bits after Header.

Configuration with status read mode

MBI6027 can report the state of configuration mode, and furthermore check if the configuration has successfully been input. Figure 29 shows the timing diagram of configuration mode status report.

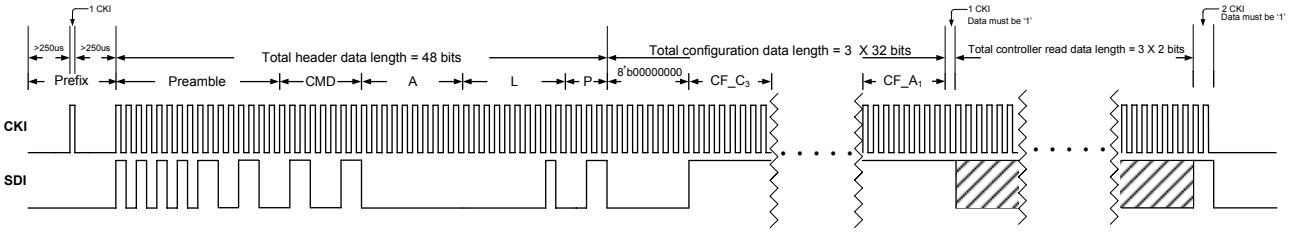

Figure 29. The timing diagram of configuration mode status report

The prefix time must be larger than 250us and be executed two successive times; the CMD[31:24] must fill in 8'b00100011. And since the L[13:4] is 2 (10'b0000000010), the data length of configuration data is 3x32 bits after Header. Finally, 1+3x2+2 bits of CKI are needed to feedback the status report to controller.

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10-bit Dot Correction Mode

Each output port of MBI6027 can execute dot correction. If GS_SEL connects to GND, the dot correction data of each output port will be 10-bit. Figure 30 shows the timing diagram of 10-bit dot correction.

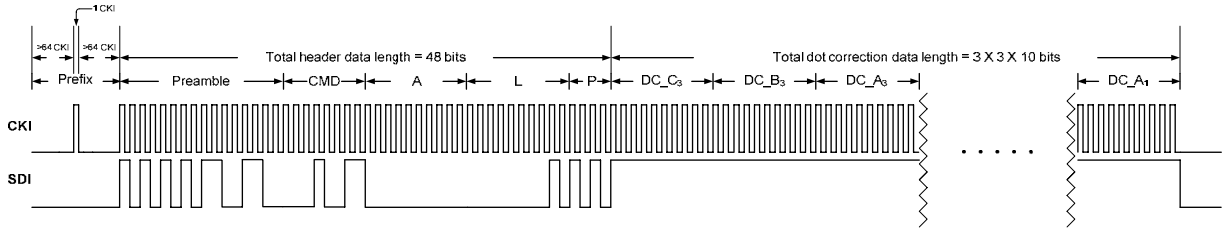

Figure 30. The timing diagram of 10-bit dot correction

The prefix time must be larger than 64-CKI and be executed two successive times; the CMD[31:24] must fill in 8'b00100011. And since the L[13:4] is 2 (10'b0000000010), the data length of dot correction data is 3x3x10 bits after Header.

10-bit Dot Correction with Status Read Mode

MBI6027 can report the state of dot correction, and furthermore check if the dot correction has successfully been input. Figure 31 shows the timing diagram of dot correction status report.

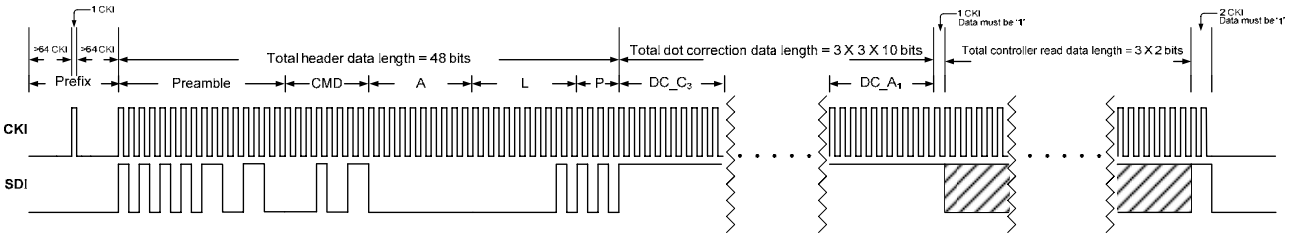

Figure 31. The timing diagram of 10-bits dot correction status report

The prefix time must be larger than 64-CKI and be executed two successive times; the CMD[31:24] must fill in 8'b01010011. And since the L[13:4] is 2 (10'b0000000010), the data length of dot correction data is 3x3x10 bits after Header. Finally, 1+3x2+2 bits of CKI are needed to feedback the status report to controller.

12-bit Gray scale Mode

Figure 32 is the timing diagram of 12-bit gray scale mode.

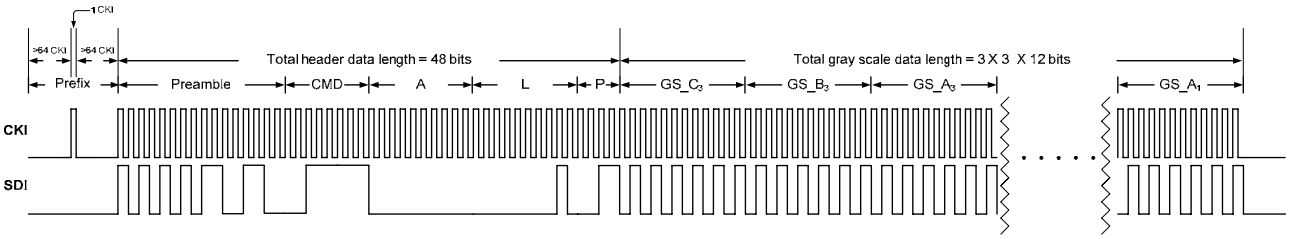

Figure 32. The timing diagram of 12-bit gray scale mode

The prefix time must be larger than 64-CKI and be executed two successive times; the CMD[31:24] must fill in 8'b00111111. And since the L[13:4] is 2 (10'b0000000010), the data length of gray scale data is 3x3x12 bits after Header.

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8-bit Dot Correction Mode

Each output port of MBI6027 can execute dot correction. If GS_SEL connect to VDD, the dot correction data of each output port will be 8-bit. Figure 33 shows the timing diagram of 8-bit dot correction.

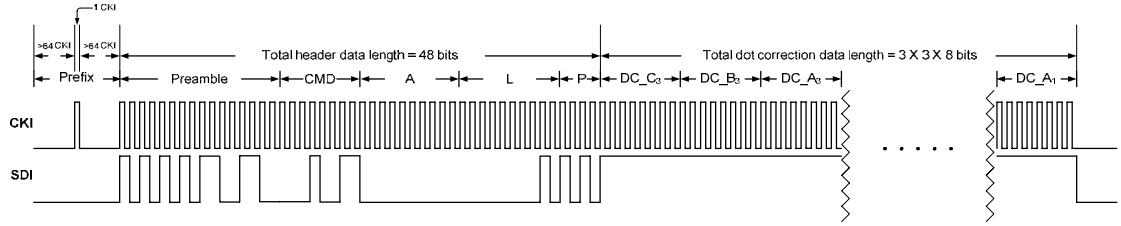

Figure 33. The timing diagram of 8-bit dot correction mode

The prefix time must be larger than 64-CKI and be executed two successive times; the CMD[31:24] must fill in 8'b00010011. And since the L[13:4] is 2 (10'b0000000010), the data length of dot correction data is 3x3x8 bits after Header.

8-bit Dot Correction with Status Read Mode

MBI6027 can report the state of dot correction, and furthermore check if the dot correction has successfully been inputted. Figure 34 shows the timing diagram of dot correction status report.

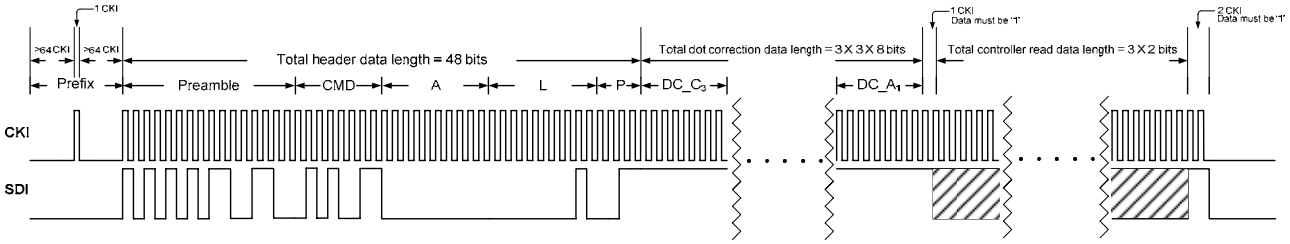

Figure 34. The timing diagram of 8-bit dot correction mode status report

The prefix time must be larger than 64-CKI and be executed two successive times; the CMD[31:24] must fill in 8'b01010011. And since the L[13:4] is 2 (10'b0000000010), the data length of dot correction data is 3x3x8 bits after Header. Finally, 1+3x2+2 bits of CKI are needed to feedback the status report to controller.

8-bit Gray Scale Mode

Figure 35 is the timing diagram of 8-bit gray scale mode.

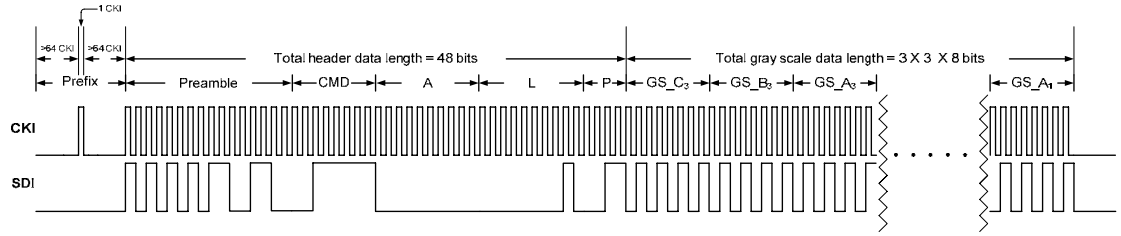

Figure 35. The timing diagram of 8-bit gray scale mode

The prefix time must be larger than 64-CKI and be executed two successive times; the CMD[31:24] must fill in 8'b00111111. And since the L[13:4] is 2 (10'b0000000010), the data length of gray scale data is 3x3x8 bits after Header.

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IC Status Report Mode

MBI6027 also features disconnect detection, /OUTx open and leakage current detection, users can execute the report mode to feedback the status to controller.

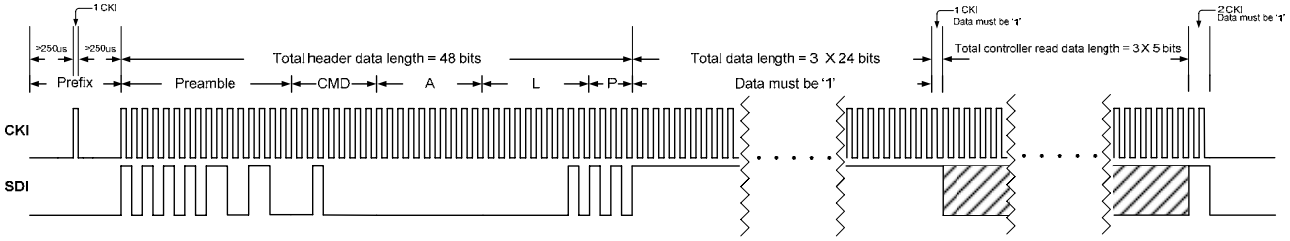

Figure 36. The timing diagram of IC status report mode

The prefix time must be larger than 250us and be executed two successive times. Since the L[13:4] is 2 (10'b0000000010), 3x24+1 bits of 1 are necessary after Header. Then 3x5 bits of CKI are required to feedback the status report to controller; and at last, 2 bits of 1 to terminate this command.

Software Reset Mode

Except the registers of dot correction and configuration, MBI6027 also provides software reset mode to reset IC's status. When the software reset mode is executed, all the output ports will be turned off, and the gray scale data has to repeat again.

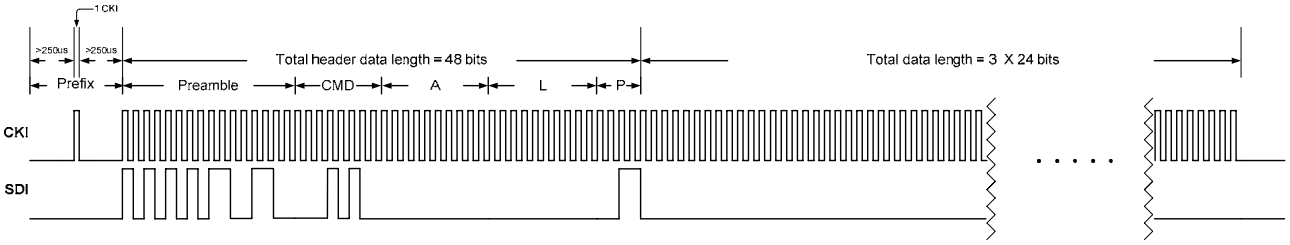

Figure 37. The timing diagram of software reset mode

The prefix time must be larger than 250us and be executed two successive times. Since the L[13:4] is 2 (10'b0000000010), 3x24+1 bits of 0 are necessary after Header.

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7. Report Data

7.1 Status Reports of Configuration Mode and Dot Correction Mode

The length of feedback data is 3x2 bits, and the sequence of status report is TE1, P1, TE2, P2, TE3 and P3. If the combination of TEn and Pn is 01, it means that the configuration or dot correction data of indicated cluster has been written successfully; otherwise means failure. Figure 38 is the timing diagram of configuration mode and dot correction status report in 3 cascaded clusters application.

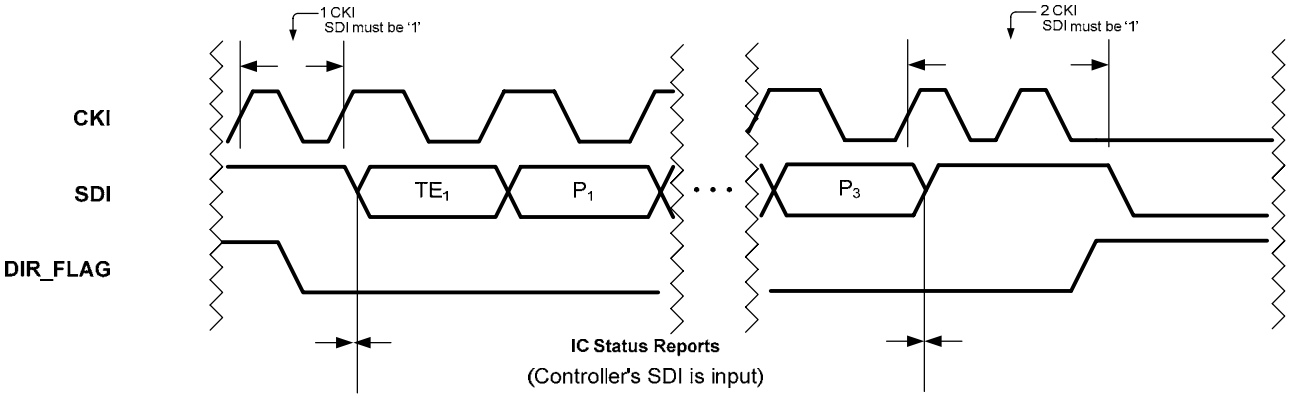

Figure 38. Timing diagram of configuration mode and dot correction status report

7.2 IC Status Repot

The length of feedback data is 3x5 bits, and the sequence of status report is $BE_1$1, $BE_0$1, OE1, LE1, P1, $BE_1$2, $BE_0$2, …, LE3 and P3. If the combination of BE_1n and BE_0n is 10, this means that the transmission of CKI/SDI works normal, otherwise means failure. Once the OEn or LEn 1 reports 1, that means the problem of LED open or output port leakage has been detected. Finally, P means the parity check used to count the amount of 1 in data string. If the amount of 1 is even, P presents 0 and 1 for odd.

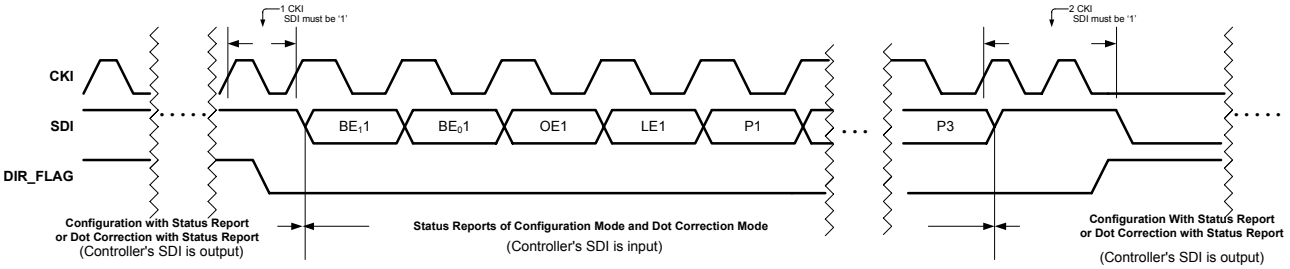

Figure 39. IC status report mode timing

The return data will be 3 x 5 bits data, with the status of a module that $BE_1$1、$BE_0$1、OE1、LE1、P1 first sent, followed by $BE_1$2、$BE_0$2…LE3 and P3. When BE_1 and BE_0 were 1 and 0 for the IC which the CKI/SDI transmission is normal, and 00,11, or 01 for the IC which the CKI/SDI transmission is not normal. When the 2-bit of OE and LE are 1, it means that IC /OUT is open or with leakage current. If that is 00, /OUT is normal. Finally, IC will send P(Parity check) and provide a value to allow the controller to change the document to determine the accuracy of the information. When the number of 1 is even, then P will be 0. When the number of 1 is odd, then P will be 1.

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III. Production and Setup

1. The Effect of Hot Swap

Hot swapping means the action of connecting or disconnecting the pin of VDD/GND/CKI/SDI/CKO/SDO of MBI6027. It will induce the heavy instantaneous current and high voltage, and then damage the IC. Besides increasing the EOS protection component as mentioned, users also may add the longer ground terminal in connectors, and operate the correct procedures to avoid hot swap.

2. Design to Reduce Strike Voltage

2.1 Resistance

Cascade a resistor at CKO and SDO can reduce the probability of IC been damaged by hot swap. The larger resistance results the lower probability of damage problem, and the lower speed of transmission. The recommended resistances of R_2 and R_3, which are shown in Figure 16, are 33Ω.

2.2 Connector

When setting up or removing the connecter of cluster instantly, in order to reduce the unexpected spike voltage and to avoid IC been burned out, users need to turn off the power, and then set up or remove the cluster. It is better to connect GND first. Users can design the longer GND terminal in connector pin than in VDD terminal in connector to reduce the unexpected strike voltage, as shown in Figure 40.

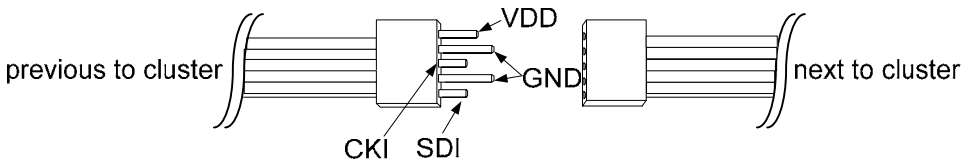

Figure 40. The safety design of power line and signal line in connectors

2.3 Transient Voltage Suppressor

All Macroblock products have passed the standard of ESD protection. But to enhance the capacity of Electrical Over Stress (EOS) protection, an external device, Transient Voltage Suppressor (TVS), is necessary. Figure 41 shows the positions of TVS_1~TVS_4, and followings are the guidelines for TVS selection.

Select TVS_1

a. The maximum Reverse Stand-Off Voltage (V_{RWM}) should be equal to module's input voltage.

b. The maximum clamping voltage (V_C) should be 1V~2V higher than module's input voltage.

c. The maximum Peak Pulsed Power (P_{PPM}) is the product of maximum clamping voltage and peak pulse current; generally, 350W is recommended.

d. TVS diode should be placed to the pins that need to protect as close as possible to prevent the EOS.

Select TVS_2

a. The maximum Reverse Stand-Off Voltage (V_{RWM}) should be equal to 5V.

b. The maximum clamping voltage (V_C) should be equal to 7V.

c. The maximum Peak Pulsed Power (P_{PPM}) is the product of maximum clamping voltage and peak pulse current; generally, 350W is recommended.

d. TVS diode should be placed to the pins that need to protect as close as possible to prevent the EOS.

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Select TVS_3 and TVS_4

a. The maximum Reverse Stand-Off Voltage (V_{RWM}) should be equal to 5V.

b. The maximum clamping voltage (V_C) should be equal to 7V.

c. The maximum Peak Pulsed Power (P_{PPM}) is the product of maximum clamping voltage and peak pulse current; generally, 350W is recommended.

d. TVS diode should be placed to the protected pins as close as possible to prevent the EOS happened.

e. For the high frequency loop, such as CKI/SDI/CKO/SDO, the parasitic capacitance of TVS will cause noise and signal attenuation. The TVS with low parasitical capacitance is adapted in high frequency application.

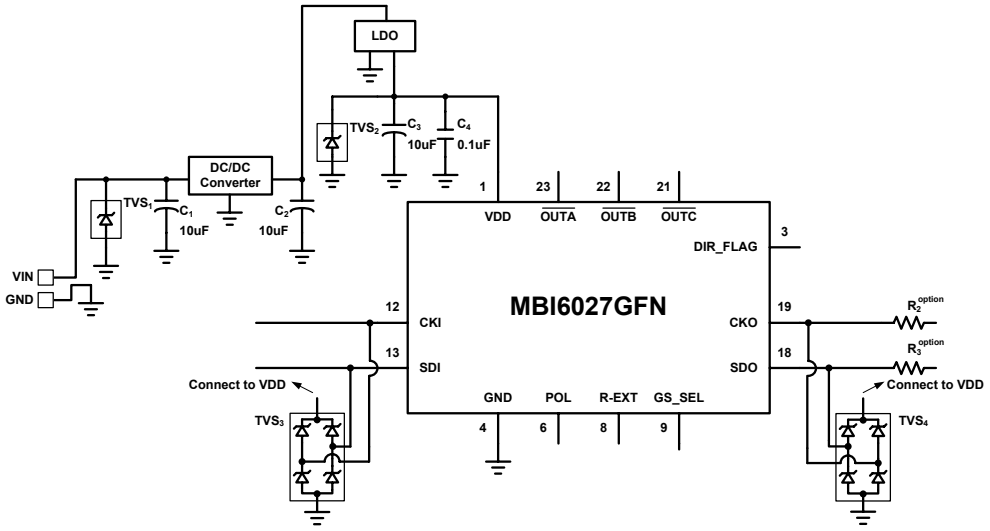

Figure 41. The Location of EOS

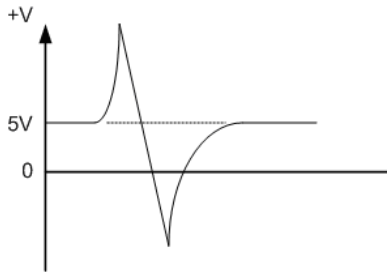

Figure 42. Without TVS

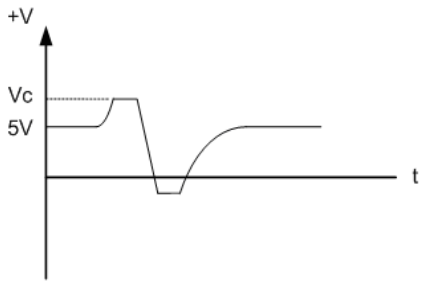

Figure 43. With TVS

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3. The Production and Installation Procedures

The following procedures should be observed in producing and installing the modules.

In order to avoid the controller from providing a valid power to the IC and cause the EOS through the ESD protection circuit. Modules in the production and installation should carefully follow the correct procedures:

Step 1: Before install the module, please turn all the power off.

Step 2: The procedure of electrostatic discharge should be taken before connecting the cluster.

Step 3: Make sure the grounding system has been properly grounded.

Step 4: Make sure all the conducting wires of power supply and controller have completed and correctly contacted with connector.

Step 5: After the above procedures have been executed, then start the system power supply.

Step 6: After the system power is stable, then start the controller power supply.

Step 7: Before the procedures of cluster removing or repairing welding, users have to turn off the controller power first and then the system power. After the residual charge has been completely discharged, then the rework procedures can be executed.

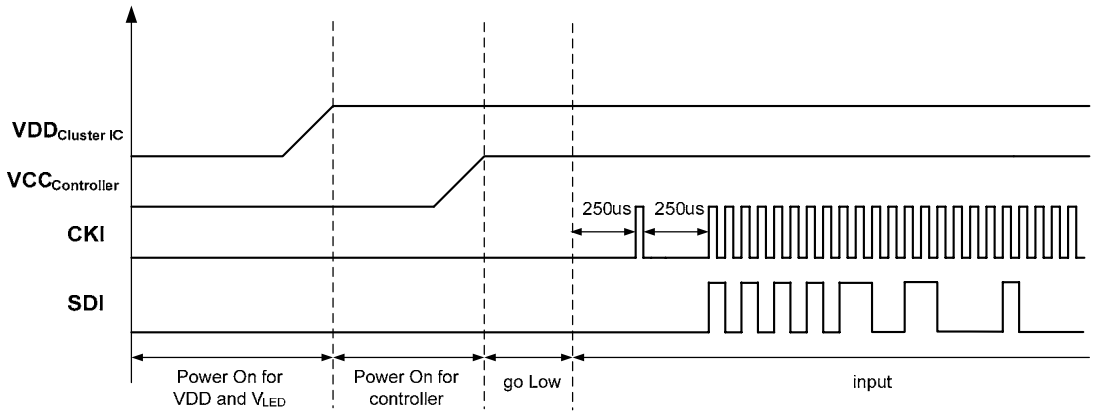

Figure 44. Power-on sequence

4. Printed Circuit Board Notice

a. Users should avoid empty solder, cold solder, and split solder in manufacturing process of printed circuit board (PCB).

b. Device layout should avoid approaching the board edge of PCB.

c. To design the longer size of PCB, it is suggested to select the thick slab value of PCB to avoid soldering issues due to board bending.

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IV. The Method of System Testing

Please use the configuration mode, dot correction mode and gray scale mode for system testing, as Figure 19 shows. The CKI frequency is 1MHz, RGB gray scale data is 10'b0101010101, and the LED turns on sequence is R→G→B→R→G…. If the LED works normally, the CKI frequency can be increased to 500kHz until LED works abnormally. If the LED can't work normally, then the CKI frequency should be decreased. The lowest CKI frequency is 200kHz. If LED still can't work under this frequency, please check if the signals of CKI and SKI have been distorted.

V: Other application Notice

1. Higher V_{LED} Application

In the more LEDs per string, if the V_{LED} is larger than the sustaining voltage of /OUT, MBI6027 might be damaged when the IC is turned off. The simplest method is to parallel a resistor (R_4~$R_{,6}$) at the output terminals of MBI6027, as shown in Figure 45. When the IC is turned off, the LED will generate a small current from the paralleled resistor, and then the V_{DS} will not exceed the sustaining voltage of output terminal.

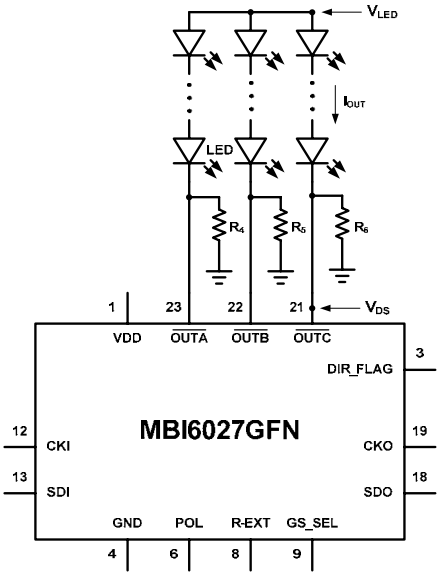

Figure 45. The application circuit of high V_{LED}.

Users can follow the steps below to calculate the paralleled resistor.

1. Find out the LED current ($I_{LED-CUT}$), which results in the invisible LED brightness.
2. Calculate the resistor

$$R_4\text{~}R_{,6} = (V_{LED} - N \times V_{F,\ LED\text{-}CUT(Max.)}) / I_{LED\text{-}CUT} \quad \text{..... (5)}$$

where N is the cascaded LED number, and $V_{F,\ LED\text{-}CUT\ (MAX)}$ is the LED forward voltage under $I_{LED\text{-}CUT}$. The calculation of $V_{LED} – N \times V_{F,\ LED\text{-}CUT\ (MAX)}$ must be smaller that the sustaining voltage of MBI6027's output terminal.

Parallel the R_4 ~ R_6 to the output terminal and turn off MBI6027. Make sure the LED brightness is invisible and V_{DS} is smaller than 17V.

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Example: The V_{LED} is 24V, and the cascaded LED number is 11. Please calculate the paralleled resistor to prevent the IC from being damaged.

Table 4. The example of LED I-V data

	Invisible lighting range						Visible lighting range							
V_F(V)	1.40	1.42	1.43	1.44	1.45	1.48	1.50	1.60	1.80	2.00	2.10	2.11	2.20	2.25
I_F(mA)	0.0003	0.0005	0.0007	0.0009	0.0011	0.0024	0.0038	0.046	2.705	12.8	19.46	20.2	26.75	30.64

1. Find out the $I_{LED-CUT}$

   Table 4 is the I-V data of the LED in this example, and the $I_{LED-CUT}$ on this table is 0.0024mA.

2. From equation (5), the R_4~R_6 are (24V – 11 x 1.48V) / 0.0024mA = 3.2MΩ. In this example, select a 3.3MΩ resistor with 0603 package to be R_4~R_6. And when IC turns off the V_{DS} should be 24V – 11 x 1.48V = 7.72V. It is smaller than 17V.

When R_4~R_6 are connected to the output terminals, and MBI6027 is turned off, the measured V_{DS} is 7.61V, and the LED current is 0.0023mA. So that the LED brightness is invisible.

2. Using the long power line on the PCB

If users have to use the long power line on the PCB, the distributed capacitors, which Figure 46 shows, are recommended. The value of C_d depends on the distance between each power line.

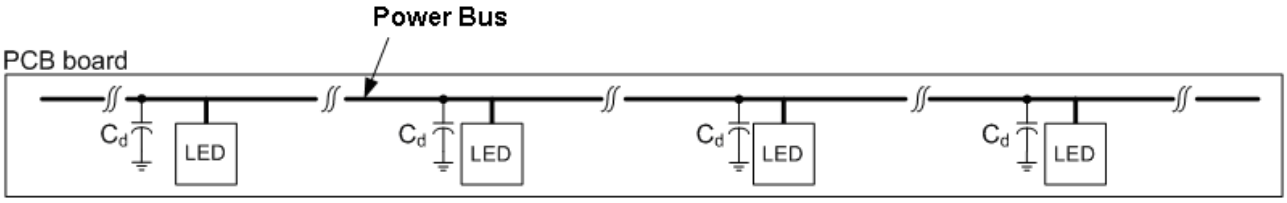

Figure 46. Distributed capacitance

3. Logic Level Issue

Due to voltage drop effect, the VDD of each cluster is different. it will lead to different logic level between clusters, as shown in Figure 47. When VDD is 5V, the V_{IH}/V_{IL} level will be 3.65V/1.4V respectively. And if the VDD of another cluster is 4V, the logic level will be 2.92V/1.12V. The different logic level will cause a different trigger time and then impact the signal transmission. Please refer to the section of "Power Configuration" for the suggested method.

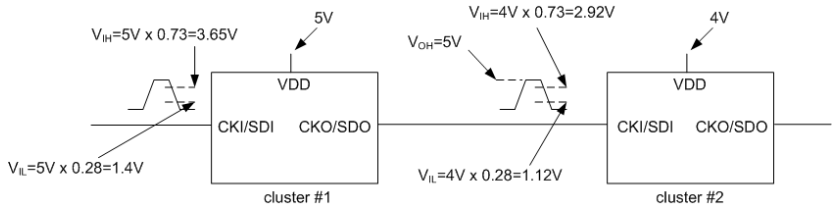

Figure 47. The diagram of different VDD

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